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SYNCHRONOUS PRESETTABLE UP/DOWN DECADA COUNTER**DESCRIPTION**

The M74LS192P is a semiconductor integrated circuit containing a synchronous decade up/down counter function with direct reset and preset inputs.

FEATURES

- Special up count, down count clock inputs
- Asynchronous preset input provided
- Direct reset input provided
- Easy cascade connection possible
- High-speed counting ($f_{max} = 38\text{MHz}$ typical)
- Wide operating temperature range ($T_a = -20 \sim +75^\circ\text{C}$)

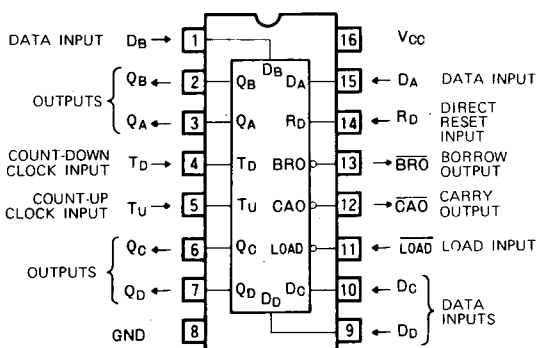
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device comes with special count-up clock input T_U and count-down clock input T_D used independently for count-up and count-down applications. For count-up, the number of count pulses appears as a BCD code in outputs Q_A , Q_B , Q_C and Q_D in synchronization with the count pulses by setting load input $\overline{LOAD}$ and T_D high, applying the count pulses to T_U while for count-down, $\overline{LOAD}$ and T_U are set high and the count pulses are applied to T_D . Counting is performed when T_U or T_D changes from low to high.

Presetting is performed independently of the count pulse. When data are applied to data inputs D_A , D_B , D_C and D_D and $\overline{LOAD}$ is set low, the D_A , D_B , D_C and D_D signals appear in the Q_A , Q_B , Q_C and Q_D outputs, respectively, regardless of the status of the T_U and T_D signals, thereby presetting the counter. Counting proceeds as per the status

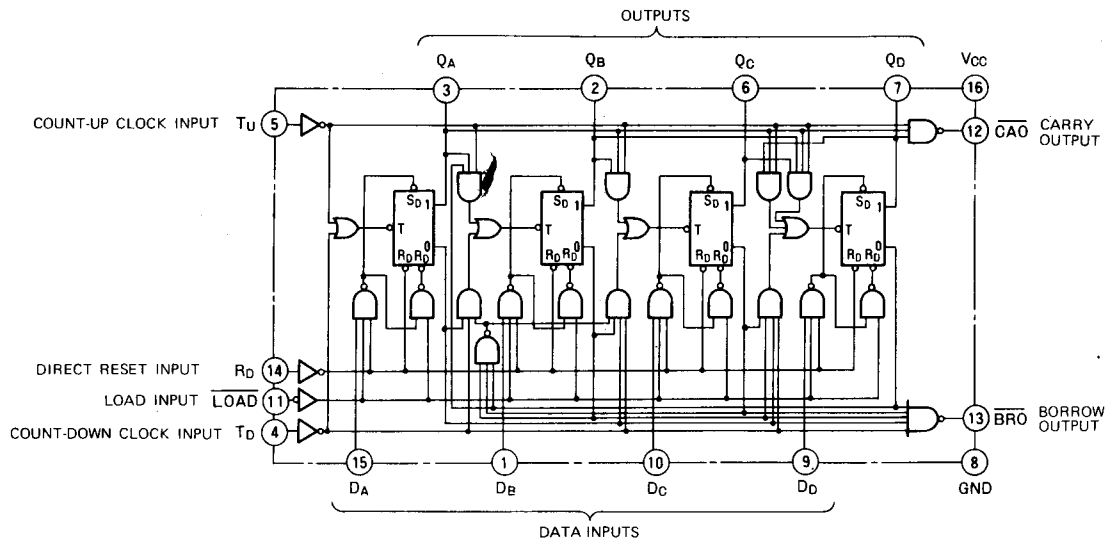
PIN CONFIGURATION (TOP VIEW)

Outline 16P4

transition diagram with presetting to a numerical value of 10 or more.

Reset can be performed by setting the direct reset input R_D high which sets $Q_A = Q_B = Q_C = Q_D$ low irrespective of the status of the other inputs.

Low appears in the carry output $\overline{CAO}$ during count-up when 9 appears in Q_A , Q_B , Q_C and Q_D and when T_U is low while low appears in output $\overline{BRO}$ when 0 appears in the outputs $\overline{CAO}$ and $\overline{BRO}$ should be connected to the next stage T_U and T_D for counter cascade connection. (Refer to the application examples.)

BLOCK DIAGRAM

SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

FUNCTION TABLE (Note 1)

R _D	LOAD	T _U	T _D	Q _A	Q _B	Q _C	Q _D	CAO	BR0
H	X	X	X	L	L	L	L	H	H*
L	L	X	X	D _A	D _B	D _C	D _D	H*	H*
L	H	H	H	Inhibit				H*	H*
L	H	↑	H	Count-up				H*	H*
L	H	H	↑	Count-down				H*	H*

Note 1. ↑ : Transition from low to high

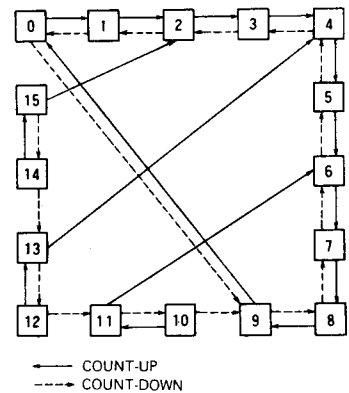
* : Normally high but low appears in accordance with the following logical expressions.

CAO = $Q_A \cdot Q_D \cdot T_U$ Count-up

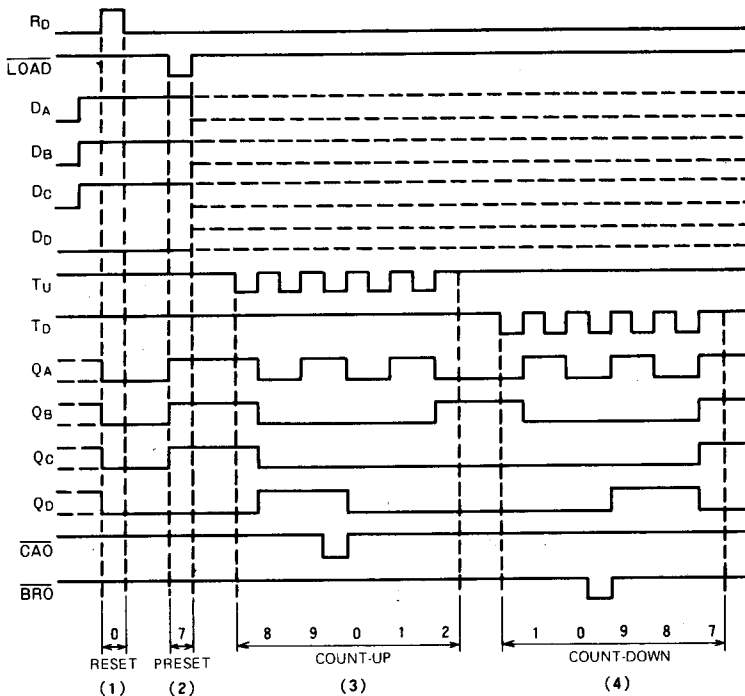
BR0 = $Q_A \cdot Q_B \cdot Q_C \cdot Q_D \cdot T_D$ Count-down

X : Irrelevant

STATE DIAGRAM



OPERATION TIMING DIAGRAM



Details of timing diagram

- (1) Reset
- (2) Preset to 7
- (3) Count-up 8, 9, 0, 1, 2
- (4) Count-down 1, 0, 9, 8, 7

ABSOLUTE MAXIMUM RATINGS (T_a = -20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V _{CC}	Supply voltage		-0.5 ~ +7	V
V _I	Input voltage		-0.5 ~ +15	V
V _O	Output voltage	High-level state	-0.5 ~ V _{CC}	V
T _{opr}	Operating free-air ambient temperature range		-20 ~ +75	°C
T _{stg}	Storage temperature range		-65 ~ +150	°C

SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

RECOMMENDED OPERATING CONDITIONS (Ta = -20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
VCC	Supply voltage		4.75	5	5.25	V
IOH	High-level output current	VOH ≥ 2.7V	0		-400	μA
IOL	Low-level output current	VOL ≤ 0.4V	0		4	mA
		VOL ≤ 0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = -20 ~ +75°C, unless otherwise noted)

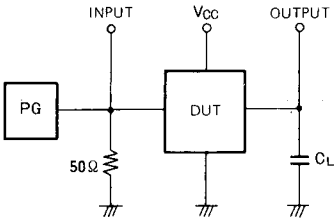
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ *	Max	
VIH	High-level input voltage		2			V
VIL	Low-level input voltage				0.8	V
VIC	Input clamp voltage	VCC = 4.75V, IIC = -18mA			-1.5	V
VOH	High-level output voltage	VCC = 4.75V, VI = 0.8V VI = 2V, IOH = -400μA	2.7	3.4		V
VOL	Low-level output voltage	VCC = 4.75V, IOL = 4mA		0.25	0.4	V
		VI = 0.8V, VI = 2V, IOL = 8mA		0.35	0.5	V
IIH	High-level input current	VCC = 5.25V, VI = 2.7V			20	μA
IIH	High-level input current	VCC = 5.25V, VI = 10V			0.1	mA
IIH	High-level input current	VCC = 5.25V, VI = 0.4V			-0.4	mA
IOS	Short-circuit output current (Note 2)	VCC = 5.25V, VO = 0V	-20		-100	mA
ICC	Supply current	VCC = 5.25V (Note 3)		19	34	mA

* : All typical values are at VCC = 5V, Ta = 25°C.
Note 2. All measurements should be done quickly and not more than one output should be shorted at a time.
Note 3. ICC is measured with RD and LOAD at 0V and TU, TD, DA~DD at 4.5V

SWITCHING CHARACTERISTICS (VCC = 5V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
fmax	Maximum clock frequency		25	38		MHz
tPLH	Low-to-high-level, high-to-low-level output propagation time, from input TU to output CA0	CL = 15pF (Note 4)		7	26	ns
tPHL	High-to-low-level output propagation time, from input TD to output BR0			14	24	ns
tPLH	Low-to-high-level, high-to-low-level output propagation time, from input TD to output BR0			7	24	ns
tPHL	High-to-low-level output propagation time, from input TU, TD to outputs QA, QB, QC, QD			19	24	ns
tPLH	Low-to-high-level, high-to-low-level output propagation time, from input TU, TD to outputs QA, QB, QC, QD			20	38	ns
tPHL	High-to-low-level output propagation time, from input TU, TD to outputs QA, QB, QC, QD			17	47	ns
tPLH	Low-to-high-level, high-to-low-level output propagation time, from input LOAD to outputs QA, QB, QC, QD			24	40	ns
tPHL	High-to-low-level output propagation time, from input LOAD to outputs QA, QB, QC, QD			20	40	ns
tPHL	High-to-low-level output propagation time, from input RD to outputs QA, QB, QC, QD			12	35	ns

Note 4. Measurement circuit



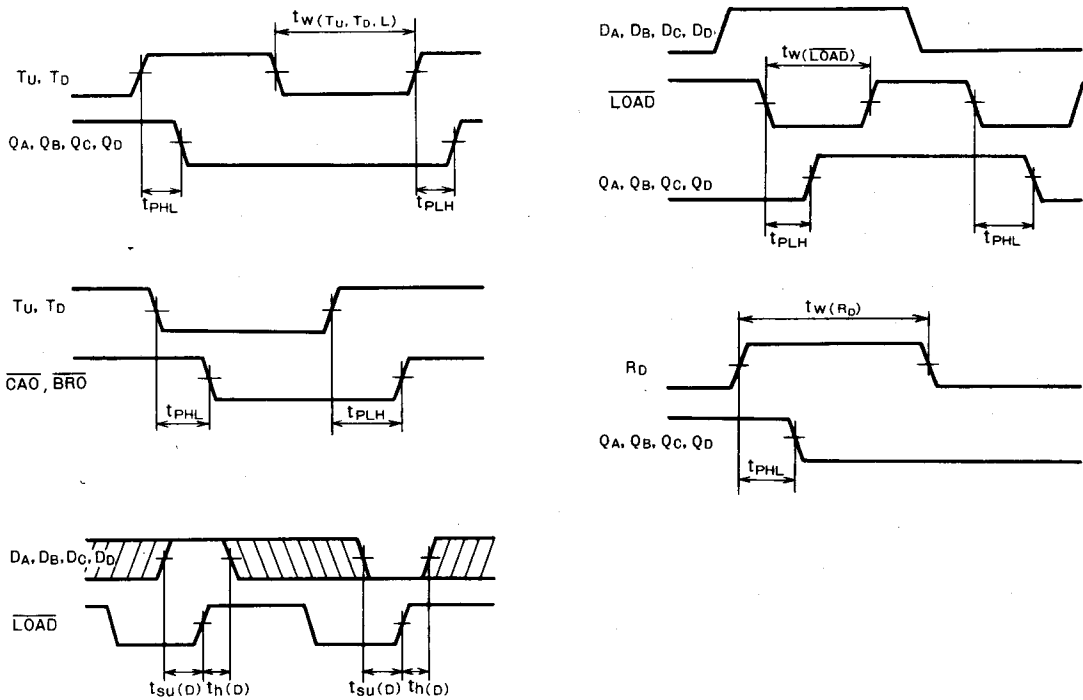
- (1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, tr = 6ns, tf = 6ns, tw = 500ns,
Vp = 3Vp.p, Zo = 50Ω.
(2) CL includes probe and jig capacitance

SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

TIMING REQUIREMENTS (V_{CC} = 5V, T_a = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t _w (T _U L)	Clock input T _U low pulse width		20	14		ns
t _w (T _D L)	Clock input T _D low pulse width		20	18		ns
t _w (LOAD)	Load LOAD pulse width		20	11		ns
t _w (R _D)	Direct reset R _D pulse width		20	4		ns
t _{SU} (D)	Setup time D _A ~D _D to LOAD		20	4		ns
t _h (D)	Hold time D _A ~D _D to LOAD		5	— 3		ns

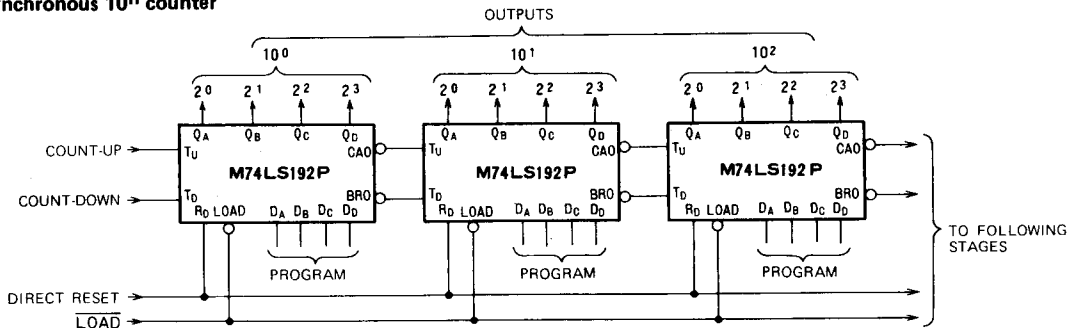
TIMING DIAGRAM (Reference level = 1.3V)



Note 5. The shaded areas indicate when the input is permitted to change for predictable output performance.

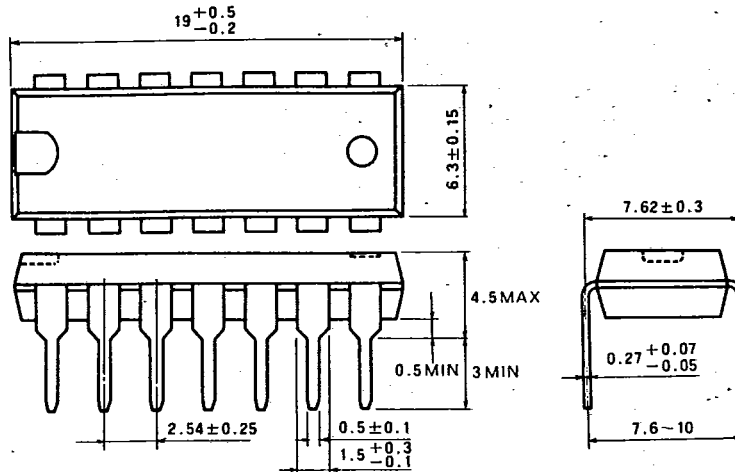
APPLICATION EXAMPLE

Asynchronous 10ⁿ counter



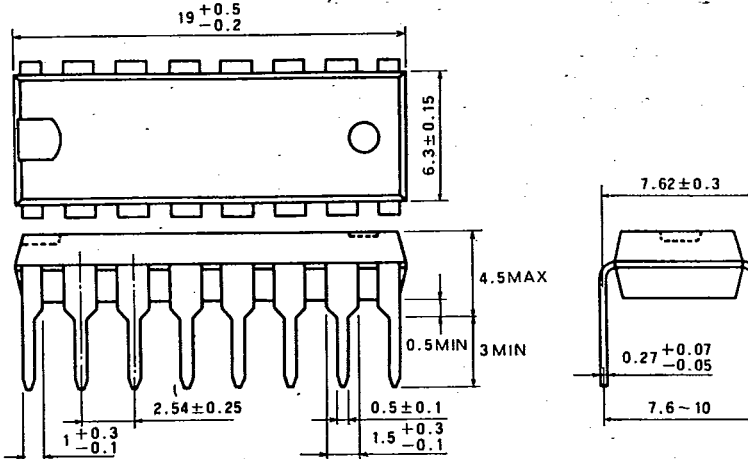
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm

